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RADIATION EVALUATION STUDY OF LSI RAM TECHNOLOGIES.(U)

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AIR FORCE WEAPONS LABORATORY
Air Force Systems Command
Kirtland Air Force Base, NM 87117

AFWL-TR-79-118

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Radiation Tests	Total Dose	

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

Five commercial LSI static RAM technologies having a 1 kilobit capacity were radiation characterized. Arrays from the TTL, Schottky TTL, NMOS, CMOS, and CMOS/SOS families were evaluated. Radiation failure thresholds for gamma dose-rate logic upset, total gamma dose survivability, and neutron fluence survivability were determined. Included is a brief analysis of the radiation failure mechanism for each of the logic families tested.

CONTENTS

ILLUSTRATIONS

I. INTRODUCTION

With the increased availability of several large-scale-integrated (LSI) static random-access-memory (RAM) technologies having a 1 kilobit capacity, system users are offered an increased potential for more radiation-tolerant memories to satisfy their individual requirements. To this end, a radiation evaluation study on five commercial static RAM arrays was undertaken. The logic families chosen for radiation characterization were: transistor-transistor-logic (TTL), Schottky TTL, n-channel metal-oxide-semiconductor (NMOS), complementary MOS (CMOS), and CMOS/silicon-on-sapphire (CMOS/SOS). Table 1 lists the specific memories chosen for this study. The RAMS were tested for gamma dose-rate logic upset and survivability, total gamma dose survivability, and neutron fluence survivability. Radiation failure thresholds for each of the five technologies are determined, and a brief analysis of the induced failure mechanism is given.

TABLE 1. SPECIFIC MEMORIES STUDIED

DEVICE NO.	MANUFACTURER	CAPACITY	TECHNOLOGY
93425DM	Fairchild	1024 x 1	TTL
S82S11F	Signetics	1024 x 1	Schottky TTL
MM2102-2MD	National	1024 x 1	NMOS
MM54C929D	National	1024 x 1	CMOS
MWS5501D	RCA	1024 x 1	CMOS/SOS

II. RAM ELECTRICAL CHARACTERIZATION

The RAMs to be tested were electrically characterized prior to being subjected to the radiation environments. Characterization was performed with the Macrodata MD-104 LSI test system. The MD-104 supplies addressing, data, and control information to the test device through an interface circuit board, and also responds to data returning from the board.

Functional operation of the RAM arrays was verified by using checkerboard, WAKPAT, and GALPAT pattern tests. The checkerboard test pattern writes an alternating 0, 1 pattern, and then reads to determine any failures. Failures are signaled on the interface board through error detection circuitry. WAKPAT (or walking pattern tests) tests all the bits, the addressing, and the interaction between the bits. A background of ones or zeros is written throughout the memory, and a testword (the background's complement) is then written in the first location of the memory. The entire memory is then read in numerical order to see that no information was disturbed. The testword is rewritten to the background state, and each succeeding location in the memory is checked in the same manner. GALPAT (or galloping ones and zeros pattern test) goes one step beyond WAKPAT, in that it tests pattern and sequence dependency for transient performance. A testword is written in the first location followed by writing the rest of the memory with the testword's complement. Then the entire memory is read in the following sequence: background location, testword, next

background, testword, etc. Each succeeding location is checked in the same manner.

In addition to the functional checks, parametric tests were performed on the RAMs to monitor the electrical degradation caused by radiation exposure. Output drive current, power supply current, and memory access times were measured at incremental radiation levels. To measure output drive currents in both the high and low states, the following (Table 2) high and low output voltage test conditions were used.

TABLE 2. HIGH AND LOW OUTPUT VOLTAGE TEST CONDITIONS

DEVICE NO.	V_{OH}(volts)	V_{OL}(volts)
93425DM	2.4	0.4
S82S11F	2.4	0.4
MM2102-2MD	2.2	0.45
MM54C929D	2.4	0.4
MWS5501D	9.5	0.5

Electrical characterization of the devices is presented in the appendixes with the radiation test data.

III. TRANSIENT RADIATION TESTS

1. TEST PROCEDURES

Gamma dose-rate tests were performed on the arrays to determine their logic upset, memory upset, and functional survivability thresholds. The tests were performed using AFWL's Febetron 705, which produces a 2 MeV flash X-ray (FXR) burst with a pulse width of 20 ns. Higher dose-rates needed for functional survivability tests were created in a 2 MeV electron-beam environment using a 50 ns burst.

Figure 1 shows the test configuration used during the FXR tests. RAMs in the radiation test environment were exercised by the Macrodata in a remote data room through the interface board and line drivers. The interface provided adjustable controls over the timing and pulse widths of the memory input signals. Line drivers insured maximum cycle rates through the 20 feet of coaxial cables to the memory arrays. A remote triggering system synchronized the FXR burst to any desired point within the memory's operating cycle. This enabled positioning of the radiation pulse at the most susceptible point in the memory's timing.

Each of the five technologies was tested in the read, write, and pause cycles. Memory upset occurs whenever memory data are lost during a radiation burst. Therefore, all three modes of operation were tested to determine the minimum radiation burst needed for upset. Logic upset occurs when the memory is irradiated in its read mode of operation, and the word(s) being immediately read cannot correctly be sensed by

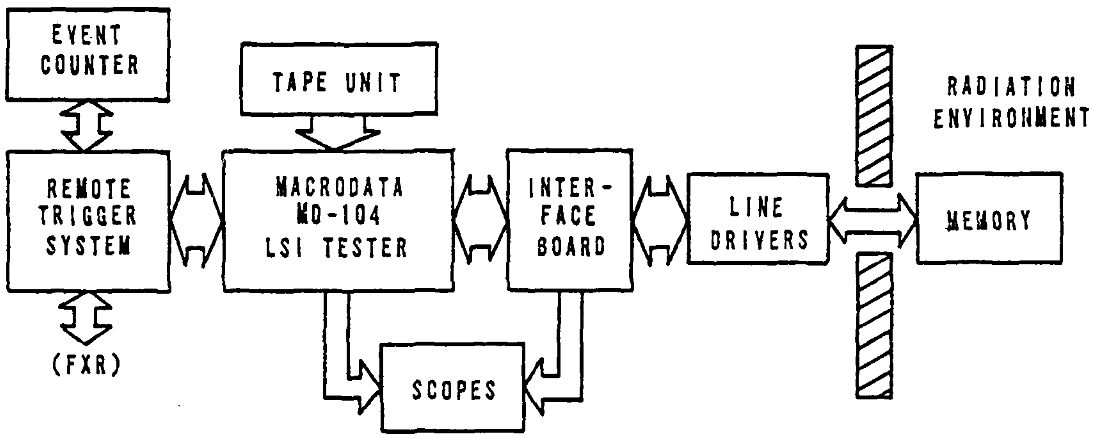


Figure 1. Block diagram of transient radiation test configuration

the TTL input of the Macrodata; actual memory data may not be lost. The functional survivability threshold is that radiation level where the device can no longer be made to functionally operate without failure.

2. TEST RESULTS

Logic and memory upset levels for each of the five technologies is listed in Table 3.

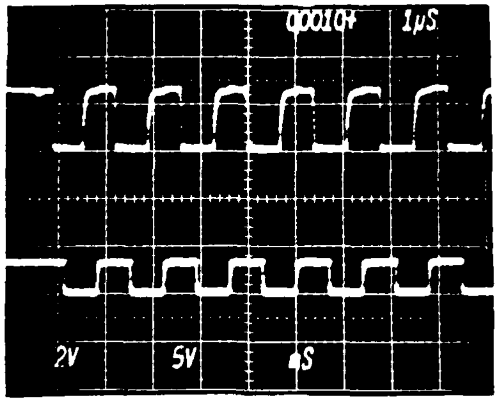
TABLE 3. LOGIC AND MEMORY UPSET LEVELS

DEVICE NO.	LOGIC UPSET THRESHOLD (L) (rads(Si)/s)	MEMORY UPSET THRESHOLD (M) (rads(Si)/s)
93425DM	$8.0 \times 10^7 < L < 2.0 \times 10^8$	$2.0 \times 10^8 < M < 4.0 \times 10^8$
S82S11F	$2.0 \times 10^7 < L < 4.0 \times 10^7$	$2.0 \times 10^8 < M < 4.0 \times 10^8$
MM2102-2MD	$9.5 \times 10^7 < L < 1.6 \times 10^8$	$9.5 \times 10^7 < M < 1.6 \times 10^8$
MM54C929D	$3.4 \times 10^7 < L < 5.0 \times 10^7$	$3.5 \times 10^7 < M < 5.0 \times 10^7$
MWS5501D	$6.0 \times 10^{10} < L < 7.0 \times 10^{10}$	$6.0 \times 10^{10} < M < 7.0 \times 10^{10}$

Both the 93425DM and S82S11F arrays were most susceptible to memory upset when irradiated during the active $R/\overline{W}$ portion of the write cycle. Memory upset levels for the three MOS devices were approximately the same in all three modes of operation. Examples of logic and memory upset are shown in Figures 2 and 3 respectively.

All the MM54C929D arrays that were FXR tested experienced latchup at 5.0×10^7 rads(Si)/s. As indicated in Figure 4, the entire memory

A. PRETEST DATA



D_{01} Output

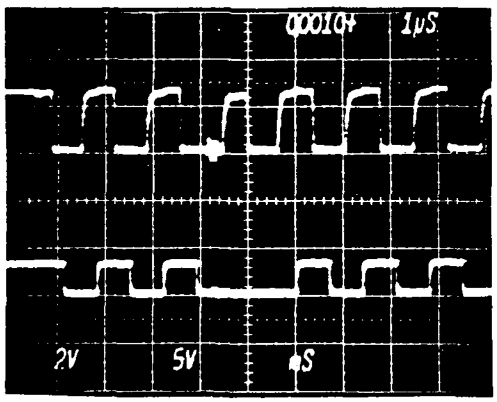
Words 1 - 13

(0101...)

MD Response

No Errors

B. POSTTEST DATA



D_{01} Output

Words 1 - 13

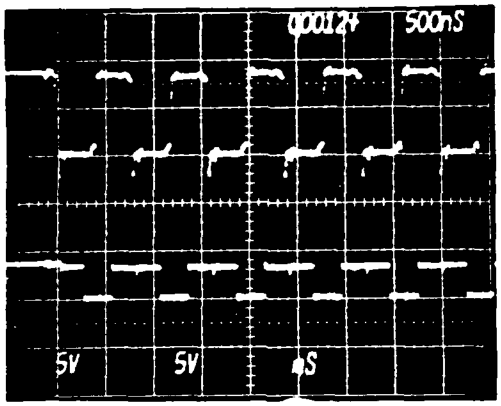
(01010?01...)

MD Response

Error Word 6

Figure 2. MM2102-2MD FXR results. Radiation burst occurs in word 6 of Read Cycle to give logic upset in word 6. A dose-rate of 1.6×10^8 rads(Si)/s was used.

A. PRETEST DATA



D_{01} Output

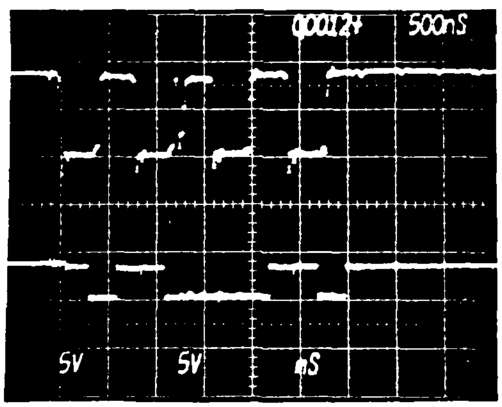
Words 1 - 11

(0101...)

MD Response

No Errors

B. POSTTEST DATA



D_{01} Output

Words 1 - 11

(0101...)

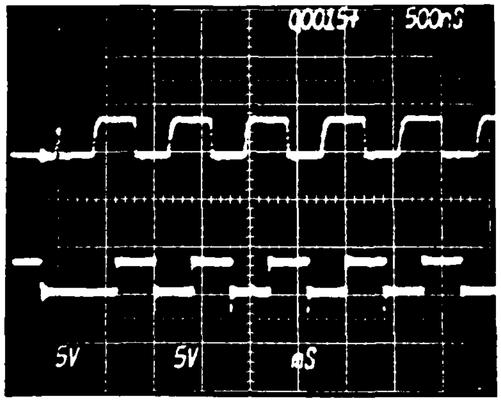
MD Response

Error Words

4, 9 - 11

Figure 3. MWS5501D FXR results. Radiation burst occurs in word 4 of the Read cycle to give logic upset in word 4 and memory loss in words 9-11. A dose-rate of 7.0 x 10^{10} rads(Si)/s was used.

A. PRETEST DATA



D_{01} Output

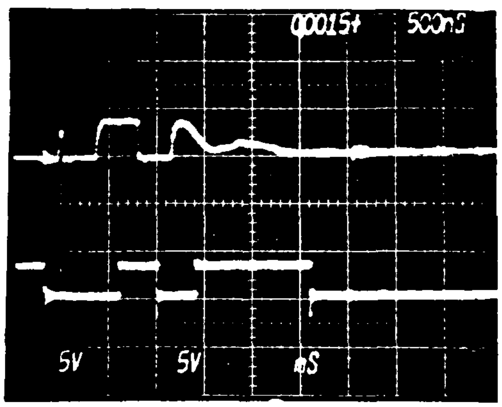
Words 1 - 11

(0101...)

MD Response

No Errors

B. POSTTEST DATA



D_{01} Output

Words 1 - 11

(0101?0?000..)

MD Response

Error Latchup

in Word 6

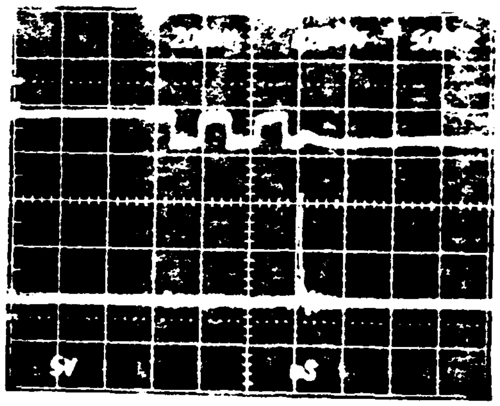
Figure 4. MM54C929D FXR results. Radiation burst occurs in word 4 of of the Read cycle. Latchup results at a dose-rate of 5.0×10^7 rads(Si)/s.

latched up in the logic 0 level. Moreover, power supply current increased from its pre-irradiation level of approximately 4 mA to 800 mA following irradiation. The 800 mA that was seen was the maximum current the power supply could deliver. Since the devices could be operated again after the power supply was turned off, latchup was not an indication of the maximum functional survivability level in this test. At a level of 2.0 x 10^{10} rads(Si)/s, two of the sixteen S82S11F arrays also latched up (Figure 5). Power supply current increased from its pre-irradiation level of 80 mA. After power was removed, the devices were again functional. The 14 remaining arrays that were tested did not experience latchup through 3.0 x 10^{12} rad(Si)/s.

In the functional survivability tests, the 93425DM and S82S11F memories were found to survive 3.0 x 10^{12} rads(Si)/s. The MWS5501D and the MM54C929D survivability failure thresholds were found to be 4.7 x 10^{11} rads(Si)/s, and the MM2102-2MD arrays became permanently disabled at 1.6 x 10^{11} rads(Si)/s. The MWS5501D and the MM54C929D failure threshold was found with the 2 MeV electron beam, 50 ns FXR pulse, whereas the MM2102-2MD failure was found with the normal 2 MeV, 20 ns FXR pulse. It is believed that failure for all of the arrays was a total dose effect rather than a dose-rate phenomenon.

Memory and logic upsets are created when the arrays are exposed to transient gamma radiation. The gamma rays generate electron-hole pairs which, in turn, cause a sudden surge in current. This photocurrent is generated in transistor pn junctions and insulators. The photocurrent flow causes changes in logic levels (logic upset) and the memory cell's stored state.

A. POSTTEST DATA



D_{01} Output

Latchup in

Word 5

FXR Burst

Figure 5. S82S11F FXR results. Radiation burst in word 5 of Read cycle. Latchup results at a dose-rate of 2.0×10^{10} rads(Si)/s.

Latchup is a transient photocurrent response in integrated circuits that can be driven into silicon controlled rectifier (SCR) action. This latchup condition is created since the mechanism in an SCR structure (Figure 6) is regenerative. To be possible in ICs, the SCR action requires that a parasitic pnpn path be present. To initiate and maintain latchup across this path, three other conditions must be met. First, the composite gain of the pnpn structure must be greater than one. Second, both end junctions of the pnpn path must be forward biased. Finally, the bias circuits which supply power to V_{DD} and the circuit inputs must be capable of supplying current equal to the holding current of the potential SCRs (Ref. 1).

Examining a typical CMOS inverter structure as shown in Figure 6, one can easily find a properly biased pnpn path. As a result, all CMOS bulk devices that satisfy the aforementioned conditions are susceptible to latchup. Although a layout of the S82S11F array was not obtained, a potential pnpn path for this technology is given in Figure 7. Fabrication process variations which affect the gain of the pnpn structure could explain why only two of the arrays experienced latchup. In NMOS memories, the fourth junction needed for SCR action is not present. Therefore, this technology is not affected by latchup. CMOS/SOS technology, too, is not troubled with latchup since it has eliminated the parasitic pnpn path. A cross-sectional view of the CMOS/SOS inverter is shown in Figure 8. The pnp and npn transistors are isolated from each other by the sapphire wafer. Fairchild's

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1. Gregory, B.L., and Shafer, B.D., "Latchup in CMOS Integrated Circuits," IEEE Trans., Vol. NS-20, No. 6, December 1973, pp. 293-299.

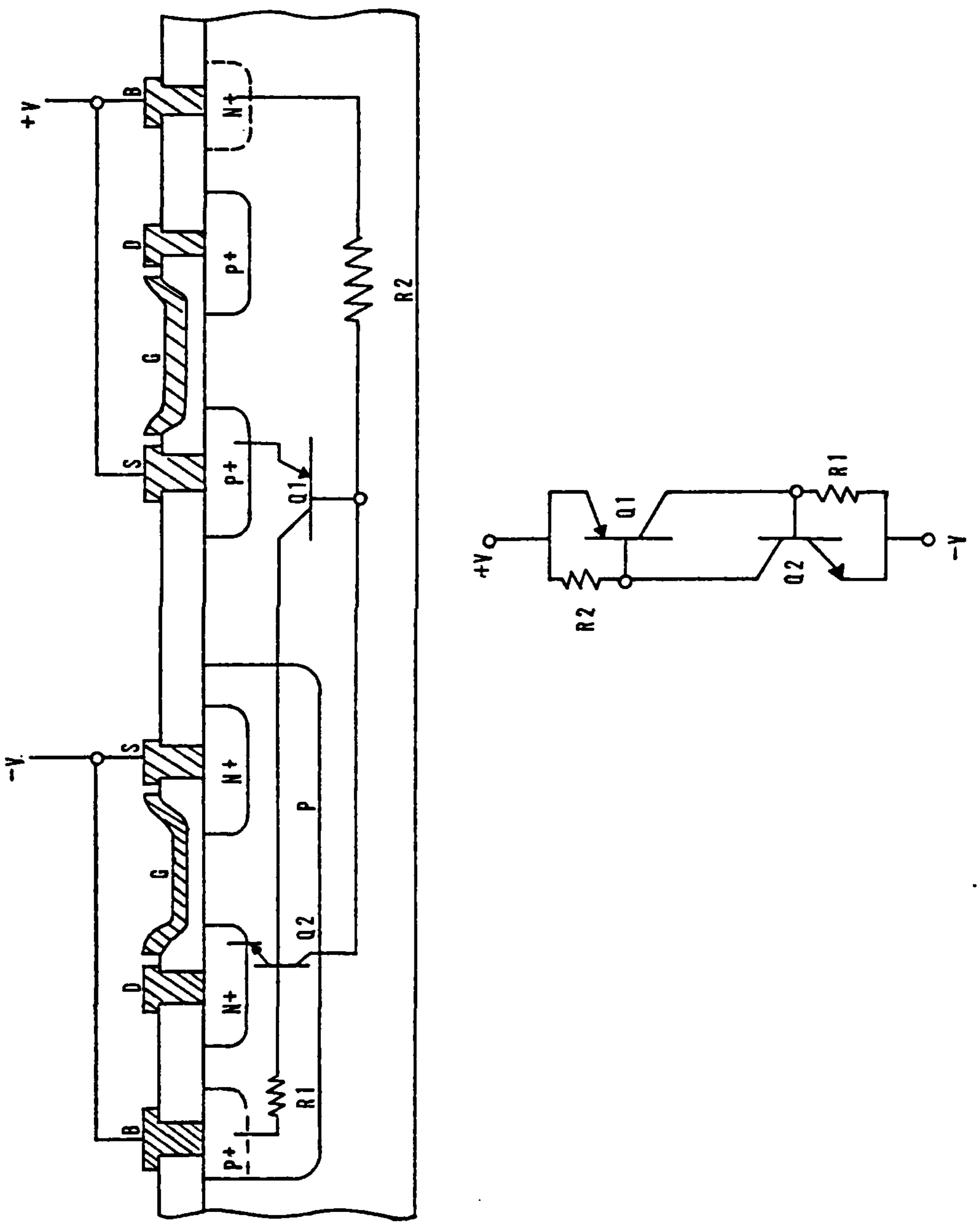

Figure 6. CMOS gate cross-section showing parasitic SCR latchup path

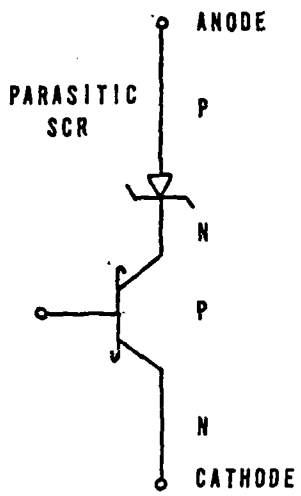

Figure 7. Potential Schottky TTL latchup path

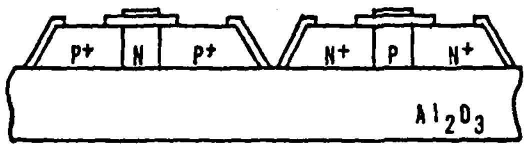

Figure 8. CMOS/SOS gate cross-section

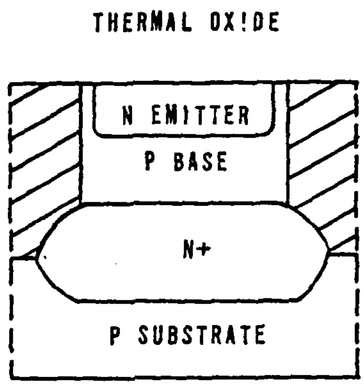

Figure 9. Isoplanar TTL transistor cross-section

Isoplaner TTL RAM, shown in Figure 9 (Ref. 2), is resistant to latchup since the transistors are isolated from each other by thermal cxide. The only available latchup is the vertical path from the substrate to emitter. The highly doped N+ layer lowers the composite gain of the pnpn structure, thereby hindering latchup. Furthermore, the substrate is grounded to prevent proper latchup biasing conditions (Ref. 3). However, a layout of the array should be obtained to ensure that there are no latchup paths resulting from crossunders or other layout considerations.

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2. Fairchild Bipolar Memory Data Book, Fairchild Camera and Instrument Corp., Mountain View, CA, 1976, pp. 4-3.

3. Crowley, J.L., Junga, F.A., and Stultz, T.S., "Techniques for Selection of Transient Radiation-Hard Junction Isolated Integrated Circuits," IEEE Trans., Vol, NS-23, No. 6, December 1976, page 1706.

IV. TOTAL GAMMA DOSE RADIATION TESTS

1. TEST PROCEDURES

Ten arrays from each of the five technologies were tested for total gamma dose survivability at AFWL's CO 60 gamma ray source. Both TTL memory types were biased with $+V_{CC}$ to the chip and ground on all inputs. Each MOS memory type had $+V_{CC}$ to the chip, however, five devices had $+V_{CC}$ to the inputs, while five devices had all inputs grounded. Incremental irradiation of 1000 rads or less were obtained at a dose-rate of 1 rad/s. For 2 krad to 5 krad irradiations, a rate of 5 rads/s was used. Increments between 10 krads and 25 krads were at a 27 rads/s rate. For increments greater than 25 krads, a rate of 195 rads/s was used. Following each incremental irradiation, the RAMs were electrically characterized and checked for functional failures.

2. TEST RESULTS

The parametric measurements taken on the 93525DM and S82S11F arrays at each incremental radiation level remained within the manufacturer's specification for that device. The arrays were incrementally irradiated from 50 krads to 1 Mrad. All 10 of both TTL memory types functionally survived the 500 krad level. At 1 Mrad, the 93425DM had seven failures out of ten, while the S82S11F had only one failure in ten. Table 4 contains average parametric measurements for each cumulative radiation level. Complete data are listed in Appendix A.

Not surprisingly, the total gamma dose functional failure thresholds for the MOS memories were considerably less than the TTL failure. All ten MM2102-MD arrays survived 500 rads(Si), but only one array

TABLE 4. AVERAGE PARAMETRIC MEASUREMENTS FROM TOTAL DOSE TESTS

93425DM

Rads(Si):	Pre	50k	100k	300k	500k	1M[a]
I_{CC1}(mA)	101.3	102.2	102.6	103.2	101.1	102.9
I_{OL}(mA)	27.2	27.3	25.8	23.4	23.3	20.1
I_{OH}(mA)	23.1	17.6	17.3	16.4	15.5	17.1
T_{AC}(ns)	20.7	21.0	22.3	24.9	25.7	23.0

S82S11F

Rads(Si):	Pre	50k	100k	300k	500k	1M[a]
I_{CC1}(mA)	81.9	81.0	81.0	79.7	78.9	76.4
I_{OL}(mA)	43.1	43.1	42.4	41.8	40.9	41.1
I_{OH}(mA)	17.4	17.5	17.4	17.3	17.2	17.6
T_{AC}(ns)	26.0	27.1	27.0	26.9	30.4	31.9

MWS5501D

Rads(Si):	Pre	5k	7k[a]	10k[a]
I_{CC2}(mA)	0.099	1.39	1.89	2.26
I_{OL}(mA)	14.4	14.2	13.5	13.0
I_{OH}(mA)	6.41	5.73	5.03	4.85
T_{AC}(ns)	77.0	74.0	75.0	81.6

a - Contains values of operational devices only.

TABLE 4. (CONTINUED)

MM2102-2MD

Rads(Si):	Pre	500
I_{CC1}(mA)	27.0	26.8
I_{OL}(mA)	1.38	1.38
I_{OH}(mA)	1.36	1.43
T_{AC}(ns)	354	350

MM54C929D

Rads(Si):	Pre	500	1500
I_{CC2}(mA)	0.076	0.976	0.565
I_{OL}(mA)	8.85	9.07	9.16
I_{OH}(mA)	6.92	6.76	6.71
T_{AC}(ns)	136	132	108

functionally survived 1500 rads(Si). Very little change in electrical performance of the arrays was seen between pre-irradiation and 500 rads(Si). Survival of the MM54C929D memories was only slightly better. While all 10 arrays functionally survived 1 krad(Si), changes in output currents and access times were noted. Nine of the ten devices functionally failed at the 3 krad(Si) level. Functional failures for MWS5501D arrays were seen as low as 7 krads(Si); all 10 devices failed at 15 krads(Si). These arrays also showed an increase in standby current. Table 4 includes the average parametric measurements for the three MOS memory types at increasing levels of gamma radiation. Complete data for these arrays are also listed in Appendix A.

Since atomic dislocations even for high energy gamma rays are not very likely, the chief mechanism for gamma-induced damage is ionization. In bipolar devices this effect can create leakage currents, but the leakages are not great enough to cause circuit failure below 10^5 rads(Si). Total ionizing dose has a more devastating effect on MOS devices. It produces a buildup of trapped positive charge in the gate-oxide insulator, and creates fast surface states at the silicon-silicon dioxide interface. The result is a marked shift in the threshold, or turn-on, voltage of the device (Ref. 4), which in turn causes failure. Charge is also known to build up in sapphire at the sapphire-silicon interface of CMOS/SOS devices. This gives rise to back channel leakage, which causes an increase in standby current.

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4. Meyers, D.K., "What Happens to Semiconductors in a Nuclear Environment?" Electronics, Vol 51, No. 6, March 16, 1978, pp. 131-133.

V. NEUTRON FLUENCE RADIATION TESTS

1. TEST PROCEDURES

Neutron fluence tests were performed at the Sandia Pulsed Neutron Reactor. Ten arrays from the TTL and Schottky TTL families were tested. As MOSFETS are inherently hard to neutron radiation, the three MOS memory types were not evaluated in the neutron environment. The arrays were irradiated from 5×10^{12} n/cm^2 to a cumulative level of 7×10^{14} n/cm^2. The fluence levels are 1 MeV equivalent. During irradiation, no electrical bias was applied to the arrays. At each level of neutron exposure, the devices were electrically characterized and checked for functional failures. Due to a testing error, five 93425DM arrays were not evaluated at 3×10^{14} n/cm^2.

2. TEST RESULTS

Output drive currents were found to decrease from pre-irradiation levels by about 30% before functional failure. Parametric and timing specifications did, however, remain within the manufacturer's specifications. Table 5 lists the average parametric test measurements and Appendix B contains complete test results. Functional test results are given below.

Neutron Fluence (n/cm^2) Functional Failures:

Device No.	5×10^{12} - 1×10^{14}	3×10^{14}	7×10^{14}
93425DM	0/10	1/10	8/10
S82S11F	0/10	1/10	7/10

TABLE 5. AVERAGE PARAMETRIC MEASUREMENTS OF NEUTRON FLUENCE TESTS

93425DM

x 10^{13} n/cm^2	Pre	0.595	4.98	12.6	31.2[a]	74.1[a]
I_{CC1}(mA)	104.0	99.1	100.9	102.2	98.6	92.5
I_{OL}(mA)	29.2	32.5	24.2	22.1	18.1	12.8
I_{OH}(mA)	28.4	18.6	18.0	19.8	17.8	17.7
T_{AC}(ns)	21.7	30.4	19.4	21.0	21.2	28.5

S82S11F

x 10^{13} n/cm^2	Pre	0.595	1.09	10.5	33.0[a]	70.0[a]
I_{CC1}(mA)	81.4	83.7	83.3	80.7	73.5	66.9
I_{OL}(mA)	44.5	43.5	43.3	37.1	30.4	29.0
I_{OH}(mA)	33.3	16.7	17.1	16.6	15.7	15.6
T_{AC}(ns)	25.9	25.8	26.9	26.9	25.9	37.3

a - Contains values of operational devices only.

The predominant neutron damage mechanism is atomic displacement. Disruption of the silicon crystal lattice structure results in generation-recombination centers which reduces minority carrier lifetime. These dislocations also decrease the mobility of both majority and minority carriers. The decrease in mobility lowers the transconductance and, therefore, the speed of the device. Reduction in minority carrier lifetime has little degrading effect on MOSFETS since they are majority carrier devices. For this reason, a neutron fluence much greater than 10^{14} n/cm^2 is needed to significantly affect MOS performance (Ref. 5). Unfortunately, this is not the case with bipolar technology. As bipolar transistors are minority carrier devices, transistor current gain (h_{FE}) is degraded and causes functional failure.

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5. Antinone, R.J., and Phillips, D. H., "A Theoretical Study of the Permanent and Transient Effects of Ionizing Radiation on the Electrical Performance of Metal Oxide Semiconductor on Sapphire Inverters," Final Report AFWL-TR-74-264, February 1976.

VI. CONCLUSIONS

This study has evaluated the radiation response of five commercially available LSI static RAM arrays. Tests for gamma dose-rate logic and memory upset revealed thresholds several orders of magnitude less than specially fabricated arrays for all the technologies except the MWS5501D CMOS/SOS arrays. The MWS5501D's threshold of 7.0×10^{10} rads(Si)/s was not surprising because of the SOS technique. However, this memory type, along with the other two MOS types, experienced a total gamma dose failure threshold on the order of 10^3 to 10^4 rads(Si); hardening techniques can significantly increase their thresholds to more than 10^6 rads(Si). Both TTL RAM arrays showed significant total dose hardness for commercial devices. Their failure thresholds were found to be greater than 5×10^5 rads(Si). Likewise, in the neutron environment, a high degree of hardness was apparent since 90% of both TTL RAM types survived 3×10^{14} n/cm^2. Latchup was seen in the MM54C929D CMOS arrays at 5.0×10^7 rads(Si)/s, but, more interestingly, the tests also found that the S82S11F Schottky TTL RAM is susceptible to latchup. Table 6 summarizes the results of this evaluation, and relates the values to typical failure thresholds of specially hardened technologies. Comparison of these values will be useful in assisting the memory design of future military and space systems subjected to radiation environments.

TABLE 6. FAILURE THRESHOLDS

COMMERCIAL TECHNOLOGY	NEUTRON (n/cm^2)	TOTAL DOSE rads(Si)	DOSE-RATE UPSET rads(Si)/s
TTL (93425DM and S82S11F)	3×10^{14}	$> 5 \times 10^{5}$	$10^{7} - 10^{8}$
NMOS (MM2102-2MD)	$> 10^{15}$	10^{3}	10^{8}
CMOS (MM54C929D)	$> 10^{15}$	$1\text{-}3 \times 10^{3}$	5×10^{7}
CMOS/SOS (MWS5501)	$> 10^{15}$	$5\text{-}7 \times 10^{3}$	7×10^{10}
HARDENED TECHNOLOGY			
TTL/DI[a]	$> 3 \times 10^{14}$	10^{6}	$10^{9} - 10^{10}$
CMOS	$> 10^{15}$	$10^{5} - 10^{6}$	$10^{8} - 10^{9}$
CMOS/SOS	$> 10^{15}$	$10^{5} - 10^{6}$	$10^{9} - 10^{10}$

a - For SSI/MSI logic only.

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4. Meyers, D.K., "What Happens to Semiconductors in a Nuclear Environment?" Electronics, Vol. 51, No. 6, March 16, 1978, pp. 131-133.

5. Antinone, R.J., and Phillips, D.H., "A Theoretical Study of the Permanent and Transient Effects of Ionizing Radiation on the Electrical Performance of Metal Oxide Semiconductor on Sapphire Inverters," Final Report AFWL-TR-74-264, February 1976.

APPENDIX A

TOTAL GAMMA DOSE TEST DATA

This appendix contains the total gamma test data for all of the devices that were examined. I_{CC1} is the power supply current being delivered while the array is cycling. I_{CC2} is the standby power supply current. Cycle rates used in the tests are given below.

DEVICE NO.	CYCLE RATE (MHz)
93425DM	5
S82S11F	5
MM2102-2MD	1.25
MM54C929D	2
MWS5501D	2

93425DM

Rads(Si):	Pre	50k	100k	300k	500k	1M
Device #21						
I_{CC1}(mA)	101	102	98	95	100	F
I_{OL}(mA)	28.6	29.1	27.4	25.3	26.9	A
I_{OH}(mA)	28.1	17.6	17.4	16.6	13.6	I
T_{AC}(ns)	18	16	18	22	25	L
Device #22						
I_{CC1}(mA)	100	105	107	105	98	F
I_{OL}(mA)	23.7	23.6	22.5	21.1	21.6	A
I_{OH}(mA)	27.9	17.5	16.8	14.0	11.7	I
T_{AC}(ns)	19	16	16	27	26	L
Device #23						
I_{CC1}(mA)	102	102	102	109	107	F
I_{OL}(mA)	29.7	31.3	30.3	27.7	27.4	A
I_{OH}(mA)	27.6	17.1	16.6	11.4	12.8	I
T_{AC}(ns)	17	18	22	32	23	L

93425DM (CONTINUED)

Rads(Si):	Pre	50k	100k	300k	500k	1M
Device #24						
I_{CC1}(mA)	101	98	100	107	95	F
I_{OL}(mA)	33.6	37.1	35.9	33.1	33.0	A
I_{OH}(mA)	28.9	18.3	18.3	18.2	17.1	I
T_{AC}(ns)	37	39	37	35	42	L
Device #25						
I_{CC1}(mA)	102	102	105	105	102	F
I_{OL}(mA)	15.6	21.9	20.7	19.3	19.2	A
I_{OH}(mA)	28.9	17.4	17.3	16.9	15.9	I
T_{AC}(ns)	17	19	18	18	23	L
Device #26						
I_{CC1}(mA)	110.2	111.4	110.5	110.0	108.8	109.3
I_{OL}(mA)	35.1	31.8	30.7	28.3	25.4	23.6
I_{OH}(mA)	17.8	17.8	17.5	17.1	17.3	17.1
T_{AC}(ns)	19	21	22	22	23	23

93425DM (CONTINUED)

Rads(Si):	Pre	50k	100k	300k	500k	1M
Device #27						
I_{CC1}(mA)	96.7	98.1	97.1	96.4	95.5	F
I_{OL}(mA)	26.3	23.6	22.7	20.5	18.3	A
I_{OH}(mA)	17.8	17.8	17.1	17.3	16.6	I
T_{AC}(ns)	18	20	22	22	23	L
Device #28						
I_{CC1}(mA)	98.3	100.7	102.4	103.1	104.3	F
I_{OL}(mA)	28.6	26.4	25.1	23.4	22.2	A
I_{OH}(mA)	17.9	17.8	17.4	17.4	16.0	I
T_{AC}(ns)	21	21	23	23	24	L
Device #29						
I_{CC1}(mA)	99	100.5	100	100.7	100.2	99
I_{OL}(mA)	25.4	23.7	23.4	20.7	19.3	18.4
I_{OH}(mA)	17.9	17.5	17.3	17.4	17.0	17.2
T_{AC}(ns)	21	20	22	23	23	23

94325DM (CONTINUED)

Rads(Si):	Pre	50k	100k	300k	500k	1M
Device #1						
I_{CC1}(mA)	102.9	102.1	103.6	100.7	100.7	100.5
I_{OL}(mA)	25.4	24.2	23.0	20.9	19.3	18.3
I_{OH}(mA)	17.9	17.4	17.4	17.4	17.1	16.9
T_{AC}(ns)	20	20	23	23	23	23

S82S11F

Rads(Si):	Pre	50k	100k	300k	500k	1M
Device #1						
I_{CC1}(mA)	79.1	79.6	78.9	77.5	76.8	75.4
I_{OL}(mA)	33.6	33.9	33.6	33.3	33.4	32.6
I_{OH}(mA)	15.7	17.0	16.9	16.9	16.6	16.8
T_{AC}(ns)	28	29	28	28	32	35
Device #2						
I_{CC1}(mA)	81.3	77.9	80.3	78.9	77.5	76.8
I_{OL}(mA)	35.2	35.2	34.9	34.0	33.3	32.6
I_{OH}(mA)	16.1	16.5	16.0	16.5	16.2	16.4
T_{AC}(ns)	26	27	27	27	30	32
Device #3						
I_{CC1}(mA)	77.5	75.6	76.0	75.4	73.9	72.5
I_{OL}(mA)	36.3	35.8	35.2	35.2	34.9	34.6
I_{OH}(mA)	17.0	17.0	16.8	16.9	16.7	16.9
T_{AC}(ns)	27	28	28	28	32	34

S82S11F (CONTINUED)

Rads(Si):	Pre	50k	100k	300k	500k	1M
Device #4						
I_{CC1}(mA)	86.0	85.5	85.2	84.5	83.8	82.4
I_{OL}(mA)	59.4	59.0	58.0	55.1	54.3	54.4
I_{OH}(mA)	19.3	19.4	19.1	18.8	18.9	18.8
T_{AC}(ns)	23	25	25	25	28	28
Device #5						
I_{CC1}(mA)	80.7	80.4	80.3	78.9	78.2	76.8
I_{OL}(mA)	61.0	61.4	60.2	59.2	58.5	57.2
I_{OH}(mA)	20.1	19.9	19.8	20.0	19.5	19.8
T_{AC}(ns)	23	24	24	25	27	28
Device #6						
I_{CC1}(mA)	79.8	78.9	79.6	78.2	77.5	76.0
I_{OL}(mA)	59.7	59.5	58.9	58.6	55.7	55.1
I_{OH}(mA)	20.1	19.9	20.0	19.4	19.5	19.8
T_{AC}(ns)	26	26	26	26	29	30

S82S11F (CONTINUED)

Rads(Si):	Pre	50k	100k	300k	500k	1M
Device #7						
I_{CC1}(mA)	95.1	92.3	92.3	90.8	90.1	F
I_{OL}(mA)	36.3	36.8	35.6	35.7	35.0	A
I_{OH}(mA)	15.9	16.0	15.8	15.6	15.7	I
T_{AC}(ns)	27	28	28	27	31	L
Device #8						
I_{CC1}(mA)	80.2	80.3	79.6	78.2	77.5	76.0
I_{OL}(mA)	32.7	32.4	32.2	32.1	31.3	30.5
I_{OH}(mA)	14.5	14.6	14.7	14.5	14.4	14.5
T_{AC}(ns)	26	27	27	26	30	32
Device #9						
I_{CC1}(mA)	79.1	78.9	78.2	76.8	76.0	74.6
I_{OL}(mA)	35.2	36.4	34.8	34.6	33.7	33.6
I_{OH}(mA)	16.7	16.8	16.9	16.6	16.6	16.6
T_{AC}(ns)	28	28	28	29	33	35

S82S11F (CONTINUED)

Rads(Si):	Pre	50k	100k	300k	500k	1M
Device #10						
I_{CC1}(mA)	80.3	80.3	79.6	78.2	77.5	76.8
I_{OL}(mA)	41.7	41.0	40.7	39.7	39.3	39.4
I_{OH}(mA)	18.0	18.1	18.1	17.8	17.9	18.5
T_{AC}(ns)	26	29	29	28	32	33

MM2102 - 2MD

Rads(Si):	Pre	500	1500
Device #1			
I_{CC1}(mA)	25.0	25.3	F
I_{OL}(mA)	1.44	1.47	A
I_{OH}(mA)	1.50	1.56	I
T_{AC}(ns)	340	335	L
Device #3			
I_{CC1}(mA)	35.3	36.4	F
I_{OL}(mA)	1.13	1.14	A
I_{OH}(mA)	1.95	1.92	I
T_{AC}(ns)	245	235	L
Device #4			
I_{CC1}(mA)	22.4	23.4	F
I_{OL}(mA)	1.40	1.40	A
I_{OH}(mA)	1.09	1.18	I
T_{AC}(ns)	370	375	L

MM2102 - 2MD (CONTINUED)

Rads(Si):	Pre	500	1500
Device #5			
I_{CC1}(mA)	18.9	19.9	21.1
I_{OL}(mA)	1.69	1.68	1.84
I_{OH}(mA)	1.14	1.62	.89
T_{AC}(ns)	260	275	300
Device #8			
I_{CC1}(mA)	27.2	2.84	F
I_{OL}(mA)	1.32	1.32	A
I_{OH}(mA)	1.38	1.43	I
T_{AC}(ns)	325	320	L
Device #11[a]			
I_{CC1}(mA)	22.2	22.5	F
I_{OL}(mA)	1.41	1.40	A
I_{OH}(mA)	.99	1.01	I
T_{AC}(ns)	445	430	L

a - Devices with grounded inputs.

MM2102 - 2MD (CONTINUED)

Rads(Si):	Pre	500	1500
Device #12[a]			
I_{CC1}(mA)	34.2	34.3	F
I_{OL}(mA)	1.10	1.09	A
I_{OH}(mA)	1.25	1.25	I
T_{AC}(ns)	345	330	L
Device #13[a]			
I_{CC1}(mA)	18.9	19.2	F
I_{OL}(mA)	1.46	1.46	A
I_{OH}(mA)	0.974	0.966	I
T_{AC}(ns)	480	470	L
Device #14[a]			
I_{CC1}(mA)	22.8	19.8	F
I_{OL}(mA)	1.52	1.51	A
I_{OH}(mA)	1.32	1.33	I
T_{AC}(ns)	460	460	L

a Devices with grounded inputs.

MM2102 - 2MD (CONTINUED)

Rads(Si):	Pre	500	1500
Device #15			
I_{CC1}(mA)	28.9	29.8	F
I_{OL}(mA)	1.37	1.36	A
I_{OH}(mA)	1.99	1.99	I
T_{AC}(ns)	270	265	L

a - Devices with grounded inputs.

MM54C929D

Rads(Si):	Pre	500	1500	3000	5000
Device #11[a]					
I_{CC1}(mA)	4.12	4.12	4.50	F	
I_{CC2}(mA)	0.076	0.076	0.534	A	
I_{OL}(mA)	10.5	10.6	10.9	I	
I_{OH}(mA)	7.26	7.19	7.02	L	
T_{AC}(ns)	100	100	100		
Device #12[a]					
I_{CC1}(mA)	3.97	3.97	4.10	4.12	4.96
I_{CC2}(mA)	0.076	0.076	0.382	0.305	1.07
I_{OL}(mA)	9.30	9.39	9.62	9.84	9.74
I_{OH}(mA)	6.66	6.60	6.46	6.17	5.93
T_{AC}(ns)	105	110	105	105	115
Device #13[a]					
I_{CC1}(mA)	3.82	3.82	4.27	F	
I_{CC2}(mA)	0.076	0.076	0.534	A	
I_{OL}(mA)	8.12	8.21	8.35	I	
I_{OH}(mA)	7.13	7.01	6.88	L	
T_{AC}(ns)	115	115	110		

a - Devices with grounded inputs.

MM54C929D (CONTINUED)

Rads(Si):	Pre	500	1500	3000	5000
Device #14[a]					
I_{CC1}(mA)	3.74	3.74	4.10	F	
I_{CC2}(mA)	0.076	0.076	0.458	A	
I_{OL}(mA)	7.80	7.88	8.04	I	
I_{OH}(mA)	6.40	6.33	6.15	L	
T_{AC}(ns)	120	120	120		
Device #15[a]					
I_{CC1}(mA)	3.89	3.89	4.81	F	
I_{CC2}(mA)	0.076	0.076	0.916	A	
I_{OL}(mA)	8.65	8.73	8.91	I	
I_{OH}(mA)	7.62	7.01	6.56	L	
T_{AC}(ns)	110	110	105		
Device #21					
I_{CC1}(mA)	3.59	3.59	3.59	F	
I_{CC2}(mA)	0.076	0.076	0.076	A	
I_{OL}(mA)	9.33	9.53	9.83	I	
I_{OH}(mA)	7.62	7.01	6.56	L	
T_{AC}(ns)	155	145	135		

a Devices with grounded input.

MM54C929D (CONTINUED)

Rads(Si):	Pre	500	1500	3000	5000
Device #22					
I_{CC1}(mA)	3.51	3.51	3.44		
I_{CC2}(mA)	0.076	0.076	0.076		
I_{OL}(mA)	8.91	9.10	9.29		
I_{OH}(mA)	6.47	6.35	6.15		
T_{AC}(ns)	165	160	150		
Device #23					
I_{CC1}(mA)	4.05	4.05	4.05	F	
I_{CC2}(mA)	0.076	0.076	0.076	A	
I_{OL}(mA)	8.58	8.72	8.95	I	
I_{OH}(mA)	6.67	6.53	6.47	L	
T_{AC}(ns)	165	155	145		
Device #24					
I_{CC1}(mA)	3.74	3.70	3.66	F	
I_{CC2}(mA)	0.076	0.076	0.076	A	
I_{OL}(mA)	8.76	8.92	9.22	I	
I_{OH}(mA)	6.56	6.43	6.32	L	
T_{AC}(ns)	170	160	140		

MM54C929D (CONTINUED)

Rads(Si):	Pre	500	1500	3000	5000
Device #25					
I_{CC1}(mA)	3.82	3.80	3.74	F	
I_{CC2}(mA)	0.076	0.076	0.076	A	
I_{OL}(mA)	9.56	9.70	10.0	I	
I_{OH}(mA)	7.08	7.01	6.92	L	
T_{AC}(ns)	155	145	130		

MWS 5501D

Rads(Si):	Pre	5k	7k	10k	15k
Device #1					
I_{CC1}(mA)	6.56	10.4	F		
I_{CC2}(mA)	0.076	2.82	A		
I_{OL}(mA)	15.7	15.4	I		
I_{OH}(mA)	7.25	6.43	L		
T_{AC}(ns)	70	75			
Device #16					
I_{CC1}(mA)	5.95	5.95	6.18	9.47	F
I_{CC2}(mA)	0.076	0.076	0.153	1.15	A
I_{OL}(mA)	12.1	12.4	12.6	12.3	I
I_{OH}(mA)	5.13	4.82	4.36	3.73	L
T_{AC}(ns)	90	75	70	90	
Device #17					
I_{CC1}(mA)	6.87	7.71	F		
I_{CC2}(mA)	0.076	0.229	A		
I_{OL}(mA)	16.5	13.3	I		
I_{OH}(mA)	6.57	5.03	L		
T_{AC}(ns)	80	60			

MWS 5501D (CONTINUED)

Rads(Si):	Pre	5k	7k	10k	15k
Device #19					
I_{CC1}(mA)	6.49	11.1	16.4	F	
I_{CC2}(mA)	0.076	3.82	6.26	A	
I_{OL}(mA)	16.2	15.8	15.3	I	
I_{OH}(mA)	6.57	5.47	4.50	L	
T_{AC}(ns)	80	60	60		
Device #20					
I_{CC1}(mA)	6.41	7.63	11.1	22.4	F
I_{CC2}(mA)	0.076	1.15	1.30	2.14	A
I_{OL}(mA)	14.4	15.2	14.8	13.3	I
I_{OH}(mA)	6.05	5.41	5.06	4.52	L
T_{AC}(ns)	85	70	75	80	
Device #11[a]					
I_{CC1}(mA)	6.56	8.24	12.5	F	
I_{CC2}(mA)	0.305	1.53	1.95	A	
I_{OL}(mA)	11.4	11.4	10.6	I	
I_{OH}(mA)	6.12	5.47	5.05	L	
T_{AC}(ns)	75	85	80		

a - Devices with grounded inputs.

MWS 5501D (CONTINUED)

Rads(Si):	Pre	5k	7k	10k	15k
Device #12[a]					
I_{CC1}(mA)	6.30	7.25	10.5	F	
I_{CC2}(mA)	0.076	0.534	1.50	A	
I_{OL}(mA)	13.0	13.6	13.0	I	
I_{OH}(mA)	6.06	5.58	4.95	L	
T_{AC}(ns)	80	85	90		
Device #13[a]					
I_{CC1}(mA)	7.18	7.48	F		
I_{CC2}(mA)	0.076	0.687	A		
I_{OL}(mA)	16.7	16.7	I		
I_{OH}(mA)	7.61	7.12	L		
T_{AC}(ns)	65	70			
Device #14[a]					
I_{CC1}(mA)	7.02	7.02	8.20	10.50	
I_{CC2}(mA)	0.076	0.229	1.20	3.50	
I_{OL}(mA)	14.9	15.0	14.8	13.5	
I_{OH}(mA)	6.69	6.45	6.30	5.25	
T_{AC}(ns)	70	80	75	85	

a - Devices with grounded inputs.

MWS 5501D (CONTINUED)

Rads(Si):	Pre	5k	7k	10k	15k
Device #15[a]					
I_{CC1}(mA)	6.26	9.69	F		
I_{CC2}(mA)	0.076	2.80	A		
I_{OL}(mA)	13.4	13.2	I		
I_{OH}(mA)	6.02	5.53	L		
T_{AC}(ns)	75	80			

a - Devices with grounded input.

Appendix B

NEUTRON FLUENCE TEST DATA

This appendix contains the neutron fluence test data for all of the devices tested. I_{CC1} is the power supply current being delivered while the arrays are cycling at 5 MHz.

93425DM

$\times 10^{13}$ n/cm^2:	Pre	0.595	4.98	12.6	31.2	74.1
Device #7						
I_{CC1}(mA)	109	105	100	102	96	90
I_{OL}(mA)	36.5	38.3	32.6	27.7	13.6	12.8
I_{OH}(mA)	25.5	20.2	19.8	21.4	18.3	17.9
T_{AC}(ns)	24	26	22	23	23	29
Device #8						
I_{CC1}(mA)	109	100	102	109	104	95
I_{OL}(mA)	35.4	40.7	29.9	29.5	29.4	12.8
I_{OH}(mA)	30.0	19.8	19.5	21.2	18.3	17.4
T_{AC}(ns)	20	33	19	19	22	28
Device #9						
I_{CC1}(mA)	110	107	105	107	102	F
I_{OL}(mA)	28.8	31.3	22.3	20.5	20.3	A
I_{OH}(mA)	29.3	19.5	19.0	21.0	19.2	I
T_{AC}(ns)	25	36	22	32	24	L

93525DM (CONTINUED)

$\times 10^{13}$ n/cm^2:	Pre	0.595	4.98	12.6	31.2	74.1
Device #10						
I_{CC1}(mA)	101	98	98	98		F
I_{OL}(mA)	28.4	29.7	22.8	20.3		A
I_{OH}(mA)	27.0	17.5	17.1	18.8		I
T_{AC}(ns)	20	33	23	18		L
Device #11						
I_{CC1}(mA)	113	112	107	114		F
I_{OL}(mA)	31.3	35.4	29.9	23.6		A
I_{OH}(mA)	32	20.9	20.9	22.6		I
T_{AC}(ns)	33	44	23	27		L
Device #14						
I_{CC1}(mA)	102	93	100	100	99	F
I_{OL}(mA)	24.3	27.5	16.8	18.9	12.1	A
I_{OH}(mA)	28.6	17.8	16.8	18.5	16.3	I
T_{AC}(ns)	19	24	18	18	17	L

93425DM (CONTINUED)

$\times 10^{13}$ n/cm^2:	Pre	0.595	4.98	12.6	31.2	74.1
Device #16						
I_{CC1}(mA)	99	100	100	102	F	
I_{OL}(mA)	26.9	30.3	19.1	21.3	A	
I_{OH}(mA)	27.9	18.0	17.3	19.0	I	
T_{AC}(ns)	18	24	16	17	L	
Device #17						
I_{CC1}(mA)	98	93	95	100	F	
I_{OL}(mA)	27.0	30.7	23.5	21.3	A	
I_{OH}(mA)	27.6	17.5	16.4	18.3	I	
T_{AC}(ns)	18	24	17	20	L	
Device #18						
I_{CC1}(mA)	99	90	100	95	F	
I_{OL}(mA)	27.9	32.9	25.5	21.5	A	
I_{OH}(mA)	28.9	17.8	17.1	18.8	I	
T_{AC}(ns)	20	14	17	17	L	

93425DM (CONTINUED)

$\times 10^{13}$ n/cm^2:	Pre	0.595	4.98	12.6	31.2	74.1
Device #19						
I_{CC1}(mA)	100	93	102	95		F
I_{OL}(mA)	25.1	27.9	20.1	18.9		A
I_{OH}(mA)	27.3	17.1	17.0	18.8		I
T_{AC}(ns)	20	26	17	19		L

S82S11F

$\times 10^{13}$ n/cm^2:	Pre	0.569	1.09	10.5	3.30	70
Device #11						
I_{CC1}(mA)	77.0	78.9	78.9	76.8	70.4	F
I_{OL}(mA)	35.9	34.9	34.6	32.0	21.3	A
I_{OH}(mA)	16.8	16.7	16.9	16.3	14.8	I
V_{OL}(V)	0.366	0.369	0.376	0.385	0.429	L
V_{OH}(V)	3.46	3.45	3.46	3.46	3.47	
T_{AC}(ns)	28	27	28	28	28	
Device #12						
I_{CC1}(mA)	79.0	81.7	81.0	78.9	72.5	F
I_{OL}(mA)	31.3	30.4	30.8	27.9	22.9	A
I_{OH}(mA)	13.2	12.8	13.4	12.9	11.9	I
V_{OL}(V)	0.389	0.387	0.390	0.406	0.442	L
V_{OH}(V)	3.45	3.44	3.44	3.45	3.45	
T_{AC}(ns)	27	27	27	28	27	

S82S11F (CONTINUED)

$\times 10^{13} n/cm^2$:	Pre	0.569	1.09	10.5	3.30	70
Device #13						
I_{CC1}(mA)	82.9	85.9	85.2	83.1	76.1	67.3
I_{OL}(mA)	58.1	58.7	56.8	52.7	39.6	28.5
I_{OH}(mA)	18.5	17.8	18.0	17.5	16.5	15.6
V_{OL}(V)	0.307	0.308	0.308	0.324	0.346	0.368
V_{OH}(V)	3.46	3.46	3.45	3.46	3.47	3.45
T_{AC}(ns)	25	25	26	25	25	37
Device #14						
I_{CC1}(mA)	82.4	85.2	84.5	81.0	74.6	F
I_{OL}(mA)	37.0	36.4	36.4	32.9	26.0	A
I_{OH}(mA)	18.3	17.0	17.4	17.2	16.5	I
V_{OL}(V)	0.369	0.370	0.372	0.389	0.418	L
V_{OH}(V)	3.44	3.44	3.44	3.44	3.45	
T_{AC}(ns)	27	27	28	27	27	

S82S11F (CONTINUED)

$\times 10^{13}$ n/cm^2:	Pre	0.569	1.09	10.5	3.30	70
Device #15						
I_{CC1}(mA)	82.2	85.2	84.5	81.7	74.6	F
I_{OL}(mA)	34.1	33.6	32.9	30.1	23.8	A
I_{OH}(mA)	15.6	15.3	15.4	15.3	14.3	I
V_{OL}(V)	0.380	0.382	0.382	0.401	0.435	L
V_{OH}(V)	3.44	3.44	3.44	3.44	3.44	
T_{AC}(ns)	25	26	28	26	25	
Device #16						
I_{CC1}(mA)	80.8	83.8	83.1	80.3	73.2	F
I_{OL}(mA)	59.7	57.3	55.9	46.7	37.4	A
I_{OH}(mA)	18.3	17.9	18.0	17.8	16.5	I
V_{OL}(V)	0.322	0.310	0.313	0.326	0.354	L
V_{OH}(V)	3.46	3.45	3.45	3.45	3.46	
T_{AC}(ns)	25	26	26	25	25	

S82S11F (CONTINUED)

x 10^{13} n/cm^2:	Pre	0.569	1.09	10.5	3.30	70
Device #17						
I_{CC1}(mA)	81.3	81.7	81.7	78.9	71.8	F
I_{OL}(mA)	35.2	34.7	35.3	30.6	24.6	A
I_{OH}(mA)	17.1	16.5	16.8	16.5	15.5	I
V_{OL}(V)	0.380	0.380	0.383	0.399	0.432	L
V_{OH}(V)	3.45	3.44	3.44	3.44	3.44	
T_{AC}(ns)	27	27	29	27	27	
Device #18						
I_{CC1}(mA)	84.7	85.2	85.2	82.4	F	
I_{OL}(MA)	34.6	34.3	35.9	30.6	A	
I_{OH}(mA)	16.1	15.5	15.9	15.4	I	
V_{OL}(V)	0.379	0.380	0.381	0.399	L	
V_{OH}(V)	3.44	3.44	3.44	3.44		
T_{AC}(ns)	26	26	27	27		

S82S11F (CONTINUED)

$\times 10^{13}$ n/cm^2:	Pre	0.569	1.09	10.5	3.30	70
Device #19						
I_{CC1}(mA)	83.2	85.0	85.2	83.1	75.4	67.3
I_{OL}(mA)	59.7	58.2	56.8	50.8	38.1	28.6
I_{OH}(mA)	19.2	18.2	19.0	18.7	17.3	14.6
V_{OL}(V)	0.310	0.308	0.311	0.326	0.351	0.384
V_{OH}(V)	3.45	3.44	3.44	3.44	3.45	3.48
T_{AC}(ns)	25	24	26	24	25	38
Device #20						
I_{CC1}(mA)	80.7	83.8	83.8	81.0	73.2	66.0
I_{OL}(mA)	59.2	56.8	57.5	50.8	39.8	30.0
I_{OH}(mA)	19.4	19.7	19.7	18.7	17.7	16.5
V_{OL}(V)	0.317	0.319	0.318	0.331	0.353	0.379
V_{OH}(V)	3.45	3.45	3.45	3.45	3.47	3.44
T_{AC}(ns)	24	23	24	23	24	37

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